REMARKS

This Amendment and Request for Continued Examination is submitted in response to the Office Action dated March 30, 2007.

Claims 7-20 and 23 have been rejected under 35 U.S.C. §112, second paragraph. Although Applicants believe the present claims satisfy the requirements of 35 U.S.C. §112, second paragraph, claims 7-20 and 23 have been amended for the sake of expediting prosecution. Claims 7-20 and 23 have been amended as suggested by the Examiner in the final Office Action.

Claims 1, 7, 21 and 23 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,764,996 to Armstrong. Claims 1-23 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,530,875 to Wach.

The Armstrong patent is directed to a method and apparatus that is intended to overcome a limitation in the shared interrupt scheme of the PCI Local Bus Specification, Revision 2.1, in which the host CPU is required to interrogate PCI devices, a so-called "Polling Method," after receiving an interrupt request in order to determine which PCI device initiated that interrupt. (see column 1, lines 41-46).

Applicants' claims are also directed to an apparatus and method that overcomes the polling methods of the prior art and the PCI Local Bus Specification (see Applicants' specification at page 2, paragraph [0006]). Applicants respectfully reiterate that they are not attempting to claim the PCI Local Bus Specification as alleged by the Examiner on page 4 of the Office Action.

The Office Action cites column 1, lines 37-43, column 2, lines 56-67, and Figure 2 of the Armstrong patent as disclosing the claimed features. However, column 1, lines 37-43 merely describes the above-mentioned PCI Local Bus Specification. While Applicants appreciate the inclusion of figures from the applied art in the Office Action, neither the figures, the cited text nor the discussion in the Office Action discloses the claimed logic that maps each of the plurality of interrupt requests to each of the plurality of interrupt inputs of an interrupt controller.

At page 17 of the final Office Action, the Examiner states that "the interrupt sources are the PCI devices 18, 20, 22, and 24" (emphasis in the original) and the interrupt requests INTA, INTB, INTC and INTD are "originated/generated from/by each of the plurality of interrupt sources 18, 20, 22, and 24." In addition, the Examiner specifically states in the Office Action that the interrupt inputs are INTA 52, INTB 54, INTC 56 and INTD 58 as shown in Figure 2 of the Armstrong patent.

As the Examiner is aware, "[A] a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Applicants' independent claim 1 recites, in combination with other features, the step of mapping each of the interrupt requests from the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt controller that receives the interrupt requests.

As shown in Figure 2 of the Armstrong patent, interrupt request INTA from PCI Device 18 is mapped to interrupt INTA 52, as are the INTAs from each of the

other PCI Devices 20, 22 and 24. However, there is no disclosure that interrupt request INTA form the devices is mapped to any of the interrupt inputs 54, 56, and 58. As such, the patent does not disclose that each interrupt request is mapped to each interrupt input, as recited in independent claim 1. Rather, each interrupt request is only mapped to one interrupt input.

Independent claims 7, 21 and 23 recite a similar combination of features.

Applicants respectfully submit that the Armstrong patent does not expressly or inherently describe each and every element of claims 1, 7, 21 and 23. Therefore, the rejection of claims1, 7, 21 and 23 over the Armstrong patent should be withdrawn.

Claims 1-23 have been also rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,530,875 to Wach.

Applicants' independent claims substantially recite the features of mapping each of the interrupt requests from the plurality of interrupt sources to each of the plurality of interrupt inputs of an interrupt controller that receives the interrupt requests, and selectively enabling interrupt requests from each of the plurality of interrupt sources to be received at one or more of the plurality of interrupt inputs.

The Examiner at pages 6-8 asserts that the claimed plurality of interrupt inputs are represented by the plurality of storage locations GF described in the Wach patent. Applicants respectfully traverse this assertion.

As disclosed in the Wach patent, the storage locations GF are part of group register 44, which must be read by the processor 14. The Wach patent specifically states at column 6, lines 21-27:

> According to this approach, when an interrupt signal is received on line 26, the processor 14, by reading register 44, identifies which group includes the interrupt source that originated the current interrupt. Based on the determination, the processor 14 checks one, and then if necessary the other, of the two locations F which correspond to the group identified by reading register 44.

The operation of the system described in the Wach patent is different from the operation of the claimed method and apparatus. In the Wach patent, the register 44 must be read by the processor 14 in order for the interrupt source to be identified (column 6, lines 21-24 of the Wach patent). This is one of the drawbacks of the prior art identified in Applicants' specification (see paragraph [0006] of Applicants' specification). It is a drawback because the interrupt manager 38 and processor 14 must determine which interrupt source is issuing the interrupt request by polling the interrupt group in register 44. The Wach patent merely reduces the number of times the processor polls the register as described at column 6, lines 25-35.

The group register 44 of the Wach patent does not constitute an interrupt controller, as that term is employed in the context of the present invention and commonly understood by those of ordinary skill in the art. Rather, as explained above, it is a passive storage device that must be interrogated by the interrupt controller in the processor to determine the origin of an interrupt received on line 26.

To clarify the distinction between these elements, claim 1 now specifies that the interrupt controller, which has a plurality of interrupt inputs, receives interrupt requests and prioritizes the servicing of received requests. See, for example, the

specification at paragraph [0004]. It is respectfully submitted that the group register 44 of the Wach patent does not meet this definition of an interrupt controller.

Independent claim 14 recites, in combination with other features, a logical OR arranged to indicate, to the interrupt inputs of an interrupt controller that receives the interrupt requests, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs. As argued above, the Wach patent does not disclose interrupt inputs of an interrupt controller that receives the interrupt requests on which are indicated the presence of a corresponding interrupt request signal as recited in independent claim 14

Applicants' respectfully submit that the Wach patent does not disclose all of the features recited in Applicants' independent claims. Therefore, the rejections of claims 1-23 over the Wach patent should be withdrawn for at least the above reasons.

Should any questions arise in connection with this application, or should the Examiner believe a telephone conference would be helpful in resolving any remaining issues pertaining to this application, the undersigned respectfully requests that he be contacted at the number indicated below.

Respectfully submitted,
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Date: July 30, 2007

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